Amendments to the Drawings:

The attached placement sheet of drawings includes changes to Figures 11-12. Figures 11-12 have been amended to include the legend "Prior Art."

REMARKS

By this amendment, Applicants have amended Figures 11 and 12 to add the legend "Prior Art" as required by the Examiner in numbered section 3 of the Office Action.

Applicants have also amended the claims to more clearly define their invention. In particular, Applicants have amended the claims to recite the protrusion presses the wiring board toward the semiconductor chip in the area overlapping the bonding opening. See, e.g., Figure 5 and the description in the paragraph bridging pages 9 and 10 of Applicants' specification.

Entry of this amendment under 37 CFR 1.116 is requested. Initially, it is submitted the foregoing amendments place the application in condition for allowance for the reasons set forth hereinafter or, at least, in better form for consideration on appeal. Moreover, since the foregoing amendments merely clarify the configuration and/or function of the protrusion, it is submitted the foregoing amendments do not raise new issues requiring further consideration and/or search. Accordingly, entry of this amendment under 37 CFR 1.116 is proper.

Claims 1 and 2 stand rejected under 35 U.S.C. 102(b) as allegedly being clearly anticipated by U.S. Patent No. 6,157,086 to Weber. Applicants traverse this rejection and request reconsideration thereof.

The present invention relates to a mold die and to a method for manufacturing a semiconductor device by sealing, by transform mold processing using a die. The present invention can be used for sealing a semiconductor chip mounting on the surface of a wiring board via an elastic material. As shown, e.g., in Figure 2, such a wiring board has a plurality of openings including a bonding opening 4. The semiconductor chip 3 can be mounted on the surface of the wiring board via an

elastic material 2. Applicants have found that bending or distortion can be generated around the bonding the opening 4 and that any such bending or distortion may allow insulating resin which flows into the bonding opening 4 to leak into the space formed between the bottom die and the insulating substrate, as shown in Figure 11. The thin insulating substrate (101) can not bear the injection pressure from the flow of the insulating resin and may float. As a result, the insulating resin 5 may be spread over the surface of the insulating substrate 101, as shown in Figure 12, and may spread over the area of the external terminal openings 101A and flow therein causing poor electrical conduction between the external connecting terminals and the conductive pattern.

The present invention solves the problems Applicants have found with the prior art by using a die which includes a protrusion disposed around an area overlapping the bonding opening to be sealed with the insulating resin. See, e.g., Figures 3, 4, 5 and 8. The protrusion presses the wiring board toward the semiconductor chip around the area overlapping the bonding opening.

For the reasons set forth from page 9, line 16 to page 11, line 5 of the substitute specification, the use of the protrusion disposed around an area overlapping the bonding opening, especially in combination with mounting the semiconductor chip on the surface of the wiring board via an elastic material, can greatly improve yield in manufacturing the semiconductor device.

The patent to Weber discloses an integrated circuit chip package that includes an integrated circuit chip mounted on a substrate by a plurality of soldered bumps. This patent discloses that a mold compound is used for underfilling air gaps between the chip and the substrate. The integrated circuit chip package is formed by placing the chip and substrate within a mold cavity and pressing a transfer mold compound into the mold cavity. Air spaces between the integrated circuit chip and the substrate

are underfilled by the mold compound as it is pressed in between the integrated circuit chip and the substrate. Air is allowed to escape from between the chip and the substrate during the underfilling through a vent which extends through the substrate. In support of the rejection, the Examiner alleges the second die 34 of Weber to comprise a protrusion around channel 38 disposed around an area overlapping the opening 26 to be sealed with the insulating resin. See, Figures 6-8 of Weber. However, the opening 26 of Weber is a vent through which air can escape, not a bonding opening. According to the present invention, the protrusion is disposed around an area overlapping the bonding opening to be sealed with the insulating resin. Such is neither disclosed nor suggested by Weber.

Moreover, the protrusion of the present invention is especially useful when the semiconductor chip is mounted on the surface of the wiring board via an elastic material. Such is neither disclosed nor suggested by Weber. While the Examiner equates the solder bumps of Weber to the elastic material of the present invention, there is no disclosure in Weber that the solder bumps have the property of being elastic.

Moreover, the protrusion of the present invention is disposed around an area overlapping the bonding opening and the protrusion presses the wiring board toward the semiconductor chip in the area overlapping the bonding opening. No such protrusion is provided in Weber.

For the foregoing reasons, claims 1 and 2 are not anticipated by Weber.

Claims 3 and 4 stand rejected under 35 U.S.C . 103(a) as being unpatentable over Weber in view of the "Admitted Prior Art." Applicants traverse this rejection and request reconsideration thereof.

The Examiner notes the "Admitted Prior Art" discloses a wiring board having a conductive pattern electrically connected to an external electrode of the

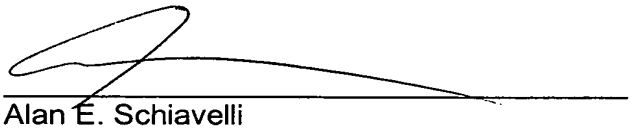
semiconductor chip in the bonding opening (referring to Figures 9 and 10). However, even assuming, arguendo, one of ordinary skill in the art would have used the transfer mold of Weber to form an integrated circuit chip package using the chip and substrate of the "Admitted Prior Art," there is no suggestion in either the "Admitted Prior Art" or in Weber to provide the protrusion around an area overlapping the bonding opening so that the protrusion presses the wiring board toward the semiconductor chip. Accordingly, claims 3 and 4 are patentable over the proposed combination of Weber and the "Admitted Prior Art."

In view of the foregoing amendments and remarks, entry of this amendment and favorable reconsideration and allowance of all of the claims now in the application are requested.

To the extent necessary, applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (Case: 501.43552X00), and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



Alan E. Schiavelli
Registration No. 32,087

AES/at
(703) 312-6600